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EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	6

DATE MAILED: 04/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,036	MICHAEL ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2-5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

> All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the manner of a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings and **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Hagersten et al (US5,864,671).

As per claim 1, Hagersten discloses a system for maintaining consistent cached copies of memory in a multi-node computing system having a main memory comprising: at least one memory directory having memory directory entries mapping the main memory [*each directory entry 602 in directory 601 corresponds to a unique memory block;* col. 7,

lines 40-43], one or more of the memory directory entries including state information for a corresponding line of main memory [*each directory entry 602 includes a field for storing the directory states of the corresponding memory blocks;* col. 7, lines 44-46]; at least one directory cache for storing directory cache lines corresponding to subset of the memory directory entries [*directory cache 604 contains directory cache entries 603 representing a subset of directory entries 602;* col. 7, lines 51-54]; and means for using the state information to allocate memory directory entries to the directory cache [*request is serviced based on whether a first node contains a valid copy of the memory block;* col. 9, lines 2-5].

As per claim 2, Hagersten discloses the use for using the state information comprises determining sharing behavior of a memory line corresponding to the state information [*request from another node can be advantageously serviced when the home node has a shared copy;* col. 15, line 57-67].

As per claim 7, Hagersten discloses the subset of memory directory entries corresponds to a set of most frequently used memory directory entries [*directory cache caches commonly used memory blocks;* col. 18, lines 1-3].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Young et al (US5,860,120).

As per claim 3, Hagersten discloses the claimed invention as detailed above in the previous paragraphs. However, Hagersten does not specifically teach the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines as recited in the claim.

Young discloses the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines [*a three bit entry indicates whether the line is cached, exclusive or shared;* col. 4, lines 34-40].

As per claim 4, Hagersten discloses the claimed invention as detailed above in the previous paragraphs. However, Hagersten does not specifically teach the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry as recited in the claim.

Young discloses the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry [*status table identifies which processors have which lines of memory in their associated caches;* col. 4, lines 20-25].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Young before him at the time the invention was made, to modify the system of Hagersten to include the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines and the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry because it would have provided an improved directory-based cache coherency memory system by reducing memory overhead requirement for the storage of memory state information [col. 1, lines 46-47, 59-60] and by reducing the amount of work that must be performed until a processor needs data that resides in a cache that cannot be accessed through snooping [col. 4, lines 25-28] as taught by Young.

6. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Guzovskiy et al (US5,752,258).

As per claim 5, Hagersten discloses the claimed invention as detailed above in the previous paragraphs. However, Hagersten does not specifically teach the state information in a memory directory entry includes a single bit indicator that indicates whether or not a memory directory entry has been accessed by multiple nodes in the multi-node computing system as recited in the claim.

Guzovskiy discloses the state information in a memory directory entry includes a single bit indicator that indicates whether or not a memory directory entry has been accessed by multiple nodes in the multi-node computing system [*state value identifies the state of access of each processor that shares access to the cache line;* col. 2, lines 39-43].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Guzovskiy before him at the time the invention was made, to modify the system of Hagersten to include the state information in a memory directory entry includes a single bit indicator that indicates whether or not a memory directory entry has been accessed by multiple nodes in the multi-node computing system because it would have allowed maximally efficient use of memory serving as fully mapped or partial mapped directory by taking action to accommodate the additional identification of processors sharing the cache line [col. 2, lines 25-27, col. 3, lines 18-19] as taught by Guzovskiy.

7. Claims 6, 19, 22-24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Smith et al (US6,055,610).

As per claims 6 and 22, Hagersten discloses the claimed invention as detailed above in the previous paragraphs. However, Hagersten does not specifically teach a multi-node system including a plurality of coherence controller subsystem wherein each of the at least one directory cache is associated with one or more of the plurality of coherence controller subsystems as recited in the claim.

Smith discloses a multi-node system including a plurality of coherence controller subsystem wherein each of the at least one directory cache is associated with one or more of the plurality of coherence controller subsystems [*fast coherency directories FD0 and FD1 associated with coherency controllers CC0 and CC1;* Fig. 1; col. 6, lines 50-54].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Smith before him at the time the invention was made, to modify the system of Hagersten to include a multi-node system including a plurality of coherence controller subsystem wherein each of the at least one directory cache is associated with one or more of the plurality of coherence controller subsystems because it would have permitted beneficial modification of the basic directory cache coding scheme by not requiring directory information regarding the presence of data in owner cell caches [col. 10, lines 32-35] as taught by Smith.

As per claim 19, Hagersten discloses the claimed invention as detailed above per claim 1 above. Hagersten further discloses a processor cache [*memory cache 702*, Fig. 7]; receiving a signal at the directory cache in one node of the system indicative of a

coherence request for a cached memory line from one of the other nodes of the system [*receiving a memory access request from a first node;* col. 8, lines 61-63]; performing a memory directory lookup to determine the location of the directory entry of the cached memory [*consulting the directory cache to determine which node possesses a copy of the memory block;* col. 9, lines 2-5]; storing information describing the sharing behavior of the cached memory line [*storing validity and state information in directory cache;* col. 17, lines 53-62].

As per claim 23, Hagersten discloses the decision to allocate is based on sharing behavior contained in the memory directory entry [*request from another node can be advantageously serviced when the home node has a shared copy;* col. 15, line 57-67].

As per claims 24 and 26, the combination of Hagersten and Smith discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Hagersten and Smith does not particularly disclose a program storage device, readable by a machine, tangibly embodying a program of instructions executable by the machine to perform the method steps of claims 19 and 22. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, CD-ROM, etc.) carrying computer executable instructions for implementing a method, because it would facilitate the transportation and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a CD-ROM from which Windows can be installed onto other systems, which is a lot easier than running a long cable or hand typing the software into another system. The examiner takes Official Notice of this

teaching. Therefore, it would have been obvious to put Hagersten and Smith's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Hagersten and Smith's program on other systems.

8. Claims 8, 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Loewenstein et al. (US6,141,692).

As per claim 8, Hagersten discloses a system for maintaining consistent cached copies of memory in a multi-node computing system having a main memory comprising: at least one memory directory having memory directory entries mapping the main memory [*each directory entry 602 in directory 601 corresponds to a unique memory block;* col. 7, lines 40-43], one or more of the memory directory entries including state information for a corresponding line of main memory [*each directory entry 602 includes a field for storing the directory states of the corresponding memory blocks;* col. 7, lines 44-46]; at least one directory cache for storing directory cache lines corresponding to subset of the memory directory entries [*directory cache 604 contains directory cache entries 603 representing a subset of directory entries 602;* col. 7, lines 51-54].

However, Hagersten does not specifically teach means for using the state information to evict directory cache lines in the directory cache as recited in the claim.

Loewenstein discloses means for using the state information to evict directory cache lines in the directory cache [*determination is made as to which cache line contains valid data before informing the home directory that the cache line is to be replaced;* col. 13, lines 17-29].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Loewenstein before him at the time the invention was made, to modify the system of Hagersten to include means for using the state information to evict directory cache lines in the directory cache because it would have provided orderly flow of memory request transactions by identifying whether the main memory in a particular node stores a copy of data found at main memory locations within other nodes [col. 12, lines 19-21; col. 14, lines 39-41] as taught by Loewenstein.

As per claim 9, Hagersten discloses the use for using the state information comprises determining sharing behavior of a memory line corresponding to the state information [*request from another node can be advantageously serviced when the home node has a shared copy;* col. 15, line 57-67].

As per claim 14, Hagersten discloses the subset of memory directory entries corresponds to a set of most frequently used memory directory entries [*directory cache caches commonly used memory blocks;* col. 18, lines 1-3].

9. Claims 10, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Loewenstein et al. (US6,141,692) and Young et al (US5,860,120).

As per claim 10, the combination of Hagersten and Loewenstein discloses the claimed invention as detailed per claim 8 above in the previous paragraphs. However, the combination of Hagersten and Loewenstein does not specifically teach the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines as recited in the claim.

Young discloses the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines [*a three bit entry indicates whether the line is cached exclusive or shared;* col. 4, lines 34-40].

As per claim 11, the combination of Hagersten and Loewenstein discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Hagersten and Loewenstein does not specifically teach the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry as recited in the claim.

Young discloses the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an

associated data cache that contains a copy of a memory line corresponding to such memory directory entry [*status table identifies which processors have which lines of memory in their associated caches;* col. 4, lines 20-25].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Loewenstein and Young before him at the time the invention was made, to modify the system of Hagersten and Loewenstein to include the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines and the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry because it would have provided an improved directory-based cache coherency memory system by reducing memory overhead requirement for the storage of memory state information [col. 1, lines 46-47, 59-60] and by reducing the amount of work that must be performed until a processor needs data that resides in a cache that cannot be accessed through snooping [col. 4, lines 25-28] as taught by Young.

10. Claims 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Loewenstein et al. (US6,141,692) and Guzovskiy et al (US5,752,258).

As per claim 12, the combination of Hagersten and Loewenstein discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Hagersten and Loewenstein does not specifically teach the state information in a memory directory entry includes a single bit indicator that indicates whether or not a memory directory entry has been accessed by multiple nodes in the multi-node computing system as recited in the claim.

Guzovskiy discloses the state information in a memory directory entry includes a single bit indicator that indicates whether or not a memory directory entry has been accessed by multiple nodes in the multi-node computing system [*state value identifies the state of access of each processor that shares access to the cache line;* col. 2, lines 39-43].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Loewenstein and Guzovskiy before him at the time the invention was made, to modify the system of Hagersten and Loewenstein to include the state information in a memory directory entry includes a single bit indicator that indicates whether or not a memory directory entry has been accessed by multiple nodes in the multi-node computing system because it would have allowed maximally efficient use of memory serving as fully mapped or partial mapped directory by taking action to accommodate the additional identification of processors sharing the cache line [col. 2, lines 25-27, col. 3, lines 18-19] as taught by Guzovskiy.

11. Claims 13, 20-21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Loewenstein et al. (US6,141,692) and Smith et al (US6,055,610).

As per claim 13, the combination of Hagersten and Loewenstein discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Hagersten and Loewenstein does not specifically teach a multi-node system including a plurality of coherence controller subsystem wherein each of the at least one directory cache is associated with one or more of the plurality of coherence controller subsystems as recited in the claim.

As per claim 20, Lowe stein discloses selecting a directory cache line for eviction based on the state information of the retrieved directory cache line [*determination is made as to which cache line contains valid data before informing the home directory that the cache line is to be replaced;* col. 13, lines 17-29]; and updating a validity indicator associated with the selected cache line to indicate that the directory cache line does not include valid information [*updating directory to reflect that node no longer contains shared copy;* col. 13, lines 30-36].

However, the combination of Hagersten and Loewenstein does not specifically teach a multi-node system including a plurality of coherence controller subsystem.

Smith discloses a multi-node system including a plurality of coherence controller subsystem wherein each of the at least one directory cache is associated with one or more of the plurality of coherence controller subsystems [*fast coherency directories FD0 and FD1 associated with coherency controllers CC0 and CC1;* Fig. 1; col. 6, lines 50-54].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Loewenstein and Smith before him at the time the invention was made, to modify the system of Hagersten and Loewenstein to include a multi-node system including a plurality of coherence controller subsystem wherein each of the at least one directory cache is associated with one or more of the plurality of coherence controller subsystems because it would have permitted beneficial modification of the basic directory cache coding scheme by not requiring directory information regarding the presence of data in owner cell caches [col. 10, lines 32-35] as taught by Smith.

As per claim 21, Loewenstein discloses examining the state information for one or more directory entries in a plurality of directory cache lines and determining sharing behavior of corresponding memory lines [*determination is made as to which cache line contains valid data (either M, O or S state);* col. 13, lines 24-26]; and selecting for eviction a directory cache line that meets a predetermined sharing behavior criterion [*each such line is to be replaced;* col. 13, lines 27-29].

As per claim 25, the combination of Hagersten and Loewenstein discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Hagersten and Loewenstein does not particularly disclose a program storage device, readable by a machine, tangibly embodying a program of instructions executable by the machine to perform the method steps of claims 19 and 22. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, CD-ROM, etc.) carrying computer executable instructions for implementing

a method, because it would facilitate the transportation and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a CD-ROM from which Windows can be installed onto other systems, which is a lot easier than running a long cable or hand typing the software into another system. The examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Hagersten and Loewenstein's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Hagersten and Loewenstein's program on other systems.

12. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Young et al (US5,860,120).

As per claim 15, Hagersten discloses a system for maintaining consistent cached copies of memory in a multi-node computing system having a main memory comprising: at least one memory directory having memory directory entries mapping the main memory [*each directory entry 602 in directory 601 corresponds to a unique memory block;* col. 7, lines 40-43].

However, Hagersten does not specifically teach the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry as recited in the claim.

Young discloses the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry [*status table identifies which processors have which lines of memory in their associated caches;* col. 4, lines 20-25].

As per claim 18, Hagersten discloses the claimed invention as detailed above in the previous paragraphs. However, Hagersten does not specifically teach the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines as recited in the claim.

Young discloses the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines [*a three bit entry indicates whether the line is cached exclusive or shared;* col. 4, lines 34-40].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Young before him at the time the invention was made, to modify the system of Hagersten to include the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines and the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to

such memory directory entry because it would have provided an improved directory-based cache coherency memory system by reducing memory overhead requirement for the storage of memory state information [col. 1, lines 46-47, 59-60] and by reducing the amount of work that must be performed until a processor needs data that resides in a cache that cannot be accessed through snooping [col. 4, lines 25-28] as taught by Young.

As per claim 16, Hagersten discloses at least one directory cache for storing directory cache lines corresponding to subset of the memory directory entries [*directory cache 604 contains directory cache entries 603 representing a subset of directory entries 602;* col. 7, lines 51-54]; and means for using the state information to allocate memory directory entries to the directory cache [*request is serviced based on whether a first node contains a valid copy of the memory block;* col. 9, lines 2-5].

As per claim 17, Hagersten discloses the use for using the state information comprises determining sharing behavior of a memory line corresponding to the state information [*request from another node can be advantageously serviced when the home node has a shared copy;* col. 15, line 57-67].

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach memory directory storing state information of memory lines, directory cache

storing cache lines corresponding to memory directory and using state information to allocate or evict directory cache lines in directory cache.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER

Pierre M. Vital
April 15, 2003